REMARKS

In the Office Action dated March 4, 2004, the final rejections have been withdrawn, with new rejections asserted against of the claims. Claims 10-15, and 20-22 were rejected under 35 U.S.C. § 102 over U.S. Patent No. 6,480,941 (Franke); and claims 1, 4-9, 16-19, 23, 24, 26, 28, 30, 32, 33, 40, and 44 were rejected under § 103 over Franke in view of Xanthaki, entitled "A Memory Controller for Access Interleaving Over a Single Rambus," dated July 1994.

Applicant acknowledges the indication that claims 25, 27, 29, 31, 34-39, and 41-43, would be allowable if rewritten in independent form.

Applicant respectfully submits that independent claim 10 is not anticipated by Franke. Claim 10 recites system that has a plurality of memory buses, and a plurality of memory controllers connected to *a first one of the memory buses*. Franke, on the other hand, describes a memory partitioning system (that provides isolation between the partitions) using a crossbar switch 200. The crossbar switch 200 has a plurality of internal buses IB (*see* Figure 2 of Franke) that are coupled to respective connector buses EC. As stated by Franke, one external connector bus can *only* be attached to one internal bus at a time. Franke, 4:61-62. "It is *imperative* that the crossbar switch *must be* programmed in such a manner that each EC_j is coupled with *at most one* IB_i to avoid a single system component (CPU, I/O Controller) being seen by more than one partition." Franke, 6:31-34. An external connector bus EC is coupled to an internal bus IB by a bus coupling device that is in the active state. Franke, 6:15-17. If the bus coupling device is in an inactive state, then the external connector bus EC is decoupled from the internal bus IB. Franke, 6:18-20. As shown in Figure 2 of Franke, one memory control interface 280 is connected to one internal bus IB--hence, there is an 1-2-1 relationship between each memory control interface 280 and a respective internal bus IB. In view of the teachings of Franke, it is clear that only one memory control interface 280 is connected to one internal bus IB, which in turn is connected to only one external connector bus EC. In the arrangement of Franke, multiple memory control interfaces *cannot* be connected to the same internal bus, as that would violate the partitioning and isolation sought by the Franke partition arrangement. *See* Franke, 1:33-39 ("In order to present to each domain the illusion of an isolated dedicated machine as well as for reasons of fault containment,

the resources of the shared-memory based multiprocessor system must then be partitioned among the several operating systems executing on these partitions."). The object of the reported invention of Franke is to provide for "flexible and secure partitioning of shared memory." Franke, 4:26-30. In this way, all system components that are attached via the bus coupling of the *same internal bus belong to a partition.* Franke, 4:62-64. Thus, providing multiple memory controllers on the same internal bus on Franke would violate the partitioning arrangement of the memory of Franke. Therefore, Franke does not disclose a subject matter of claim 10.

Moreover, the memory control interfaces 280 snoop on a respective internal bus IB for memory operations, and any such memory operation is then forwarded to a memory controller 110 for processing. The memory control interfaces do *not* monitor memory requests generated by each other. For this additional reason, Franke fails to disclose the subject matter of claim 10.

Because of the one-to-one correspondence between a memory control interface and an internal bus IB, the further element of claim 10 where the memory controllers are able to access a second one of the memory buses through a hub also cannot be satisfied by Franke. Note that claim 10 recites plural memory controllers to access *a* second one of the memory buses through the hub (in addition to being connected to *a* first one of the memory buses). Such an arrangement does not exist in Franke.

Withdrawal of the rejection of claim 10 is respectfully requested.

With respect to independent claim 15, Franke does not disclose each memory controller monitoring memory-related actions on the memory buses connected by the hub by at least another memory controller. Note that the isolation desired between the internal buses IB and the different partitions would prevent one memory controller interface from monitoring memory-related actions on another bus that the memory controller is not connected to. Therefore, Franke does not anticipate claim 15.

Independent claim 1 was rejected as being obvious over Franke and Xanthaki. With respect to independent claim 1, the Office Action asserted that Franke discloses everything in claim 1 accept the predetermined priority scheme defining time slots recited in claim 1. Applicant respectfully disagrees that Franke discloses that each of a plurality of memory controllers is able to generate memory requests on *the same* memory bus. In

Franke, memory partitioning requires that one memory control interface be connected to an individual internal bus IB. Therefore, the multiple memory control interfaces of Franke cannot generate memory requests on the same internal bus IB. Therefore, even if Franke and Xanthaki can be properly combined, the asserted combination of Franke and Xanthaki does not teach or suggest *all* elements of claim 1. Therefore, a *prima facie* case of obviousness has not been established with respect to claim 1 over Franke and Xanthaki.

Also, there did not exist any motivation or suggestion to combine Franke and Xanthaki to achieve the claimed invention. Note that Xanthaki is also concerned with *one memory controller* on *one* memory bus (a Rambus channel). *See* Xanthaki, Section 2.1, Figure 2.2. The access interleaving discussed in Xanthaki refers to interleaving access requests from *one* memory controller or master on the Rambus channel, not from plural *memory controllers on the plural Rambus channels*. Thus, a priority scheme to define access to a memory bus by *plural* memory controllers as recited in claim 1 is quite different from an access interleaving arrangement for requests by only *one* memory controller, as taught by Xanthaki. Therefore, there is no suggestion by Xanthaki of a priority scheme for defining access by multiple memory controllers on *a* memory bus. Therefore, no motivation or suggestion existed to combine Franke and Xanthaki in the manner proposed by the Office Action. A *prima facie* case of obviousness is defective for this further reason.

Independent claim 23 is allowable for reasons similar to those as for claim 1.

All dependent claims are allowable for at least the same reasons as corresponding independent claims. Therefore, allowance of all claims is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account No. 50-1673 (9295).

Respectfully submitted,

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